

FIG. 1A
(PRIOR ART)

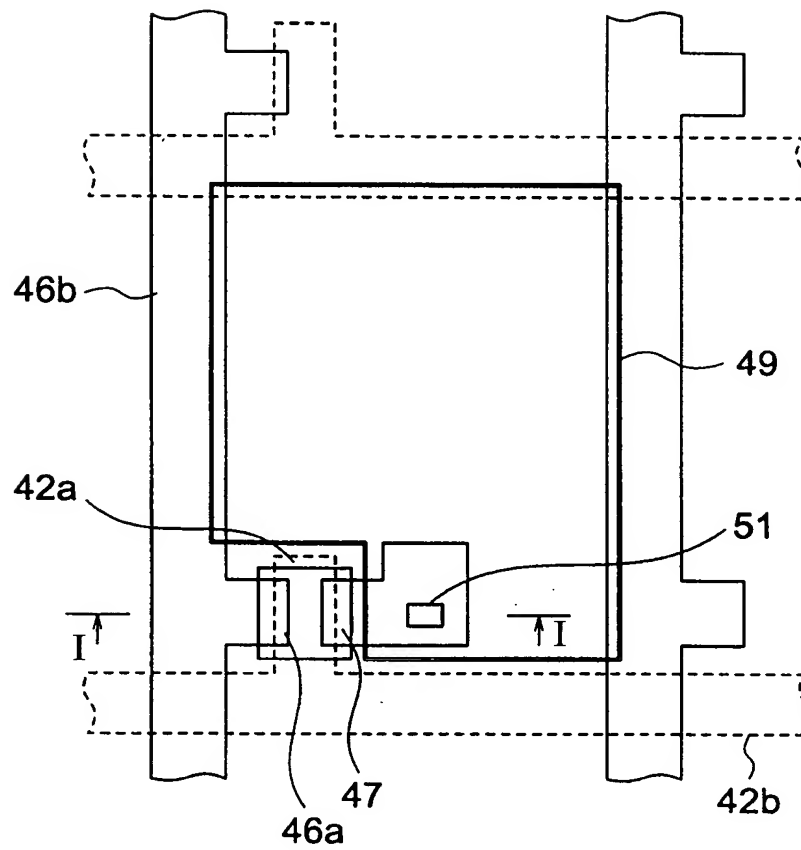


FIG. 1B
(PRIOR ART)

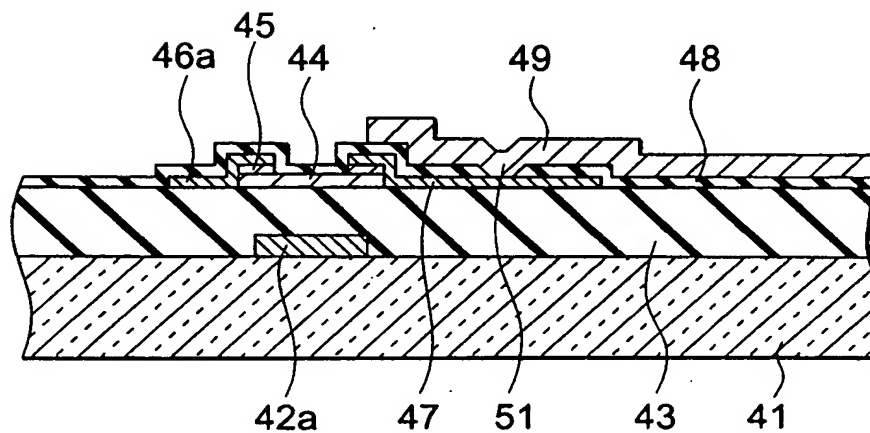


FIG. 2A
(PRIOR ART)

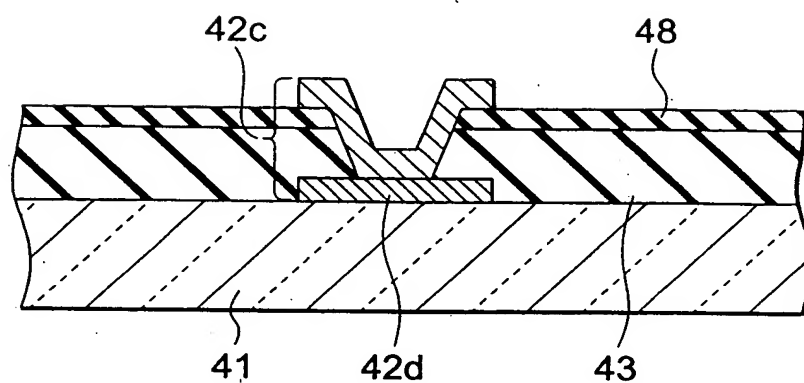


FIG. 2B
(PRIOR ART)

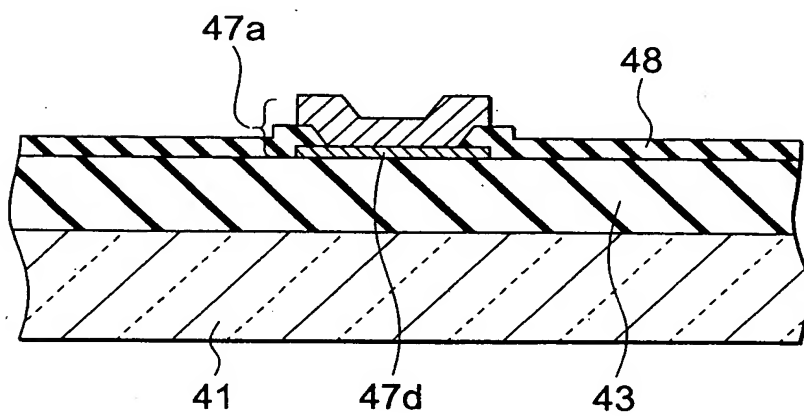


FIG. 3A
(PRIOR ART)

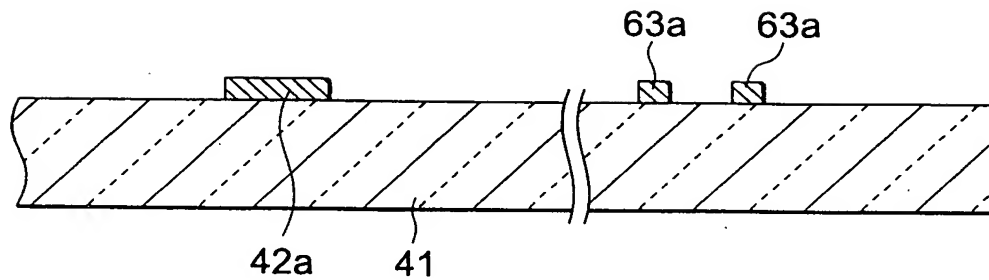


FIG. 3B
(PRIOR ART)

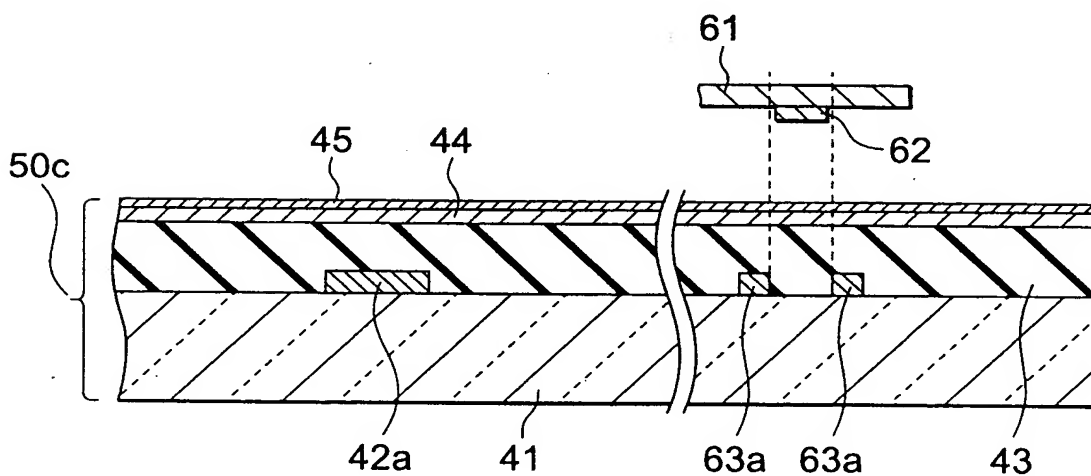
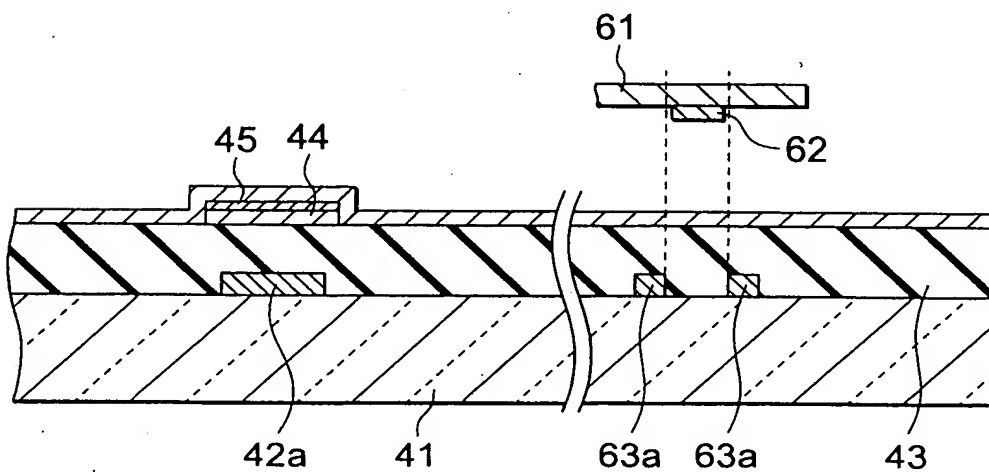


FIG. 3C
(PRIOR ART)



[illegible]

This cross-sectional view shows a semiconductor device with a gate stack (41, 42a, 47, 48, 49) and source/drain regions (43, 44, 45, 46a, 46b). The gate stack includes a gate dielectric (41), a gate insulating layer (42a), a gate electrode (47), and a gate cap (48, 49). The source/drain regions are formed in the substrate (43) and are covered by a source/drain cap (44, 45, 46a, 46b). A dashed line indicates the boundary between the gate stack and the source/drain regions. A bracket on the right side of the diagram indicates the overall thickness of the device (50c).

FIG. 5A (PRIOR ART)

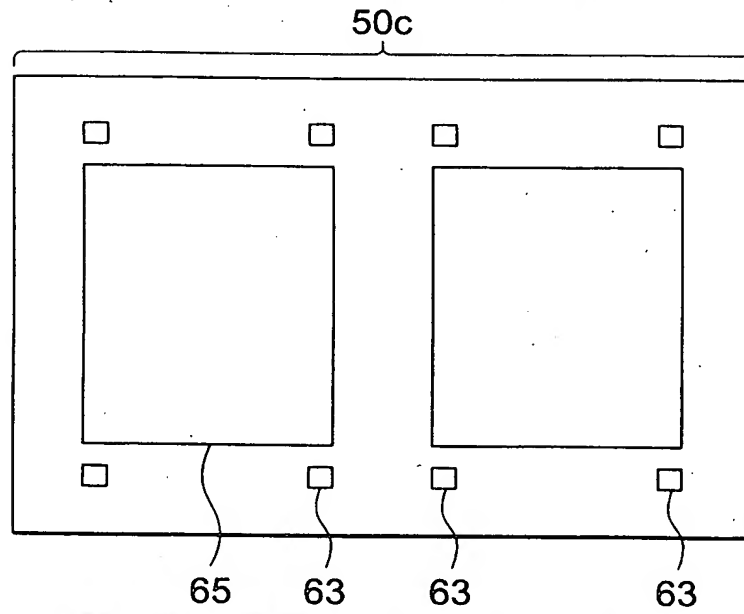


FIG. 5B (PRIOR ART)

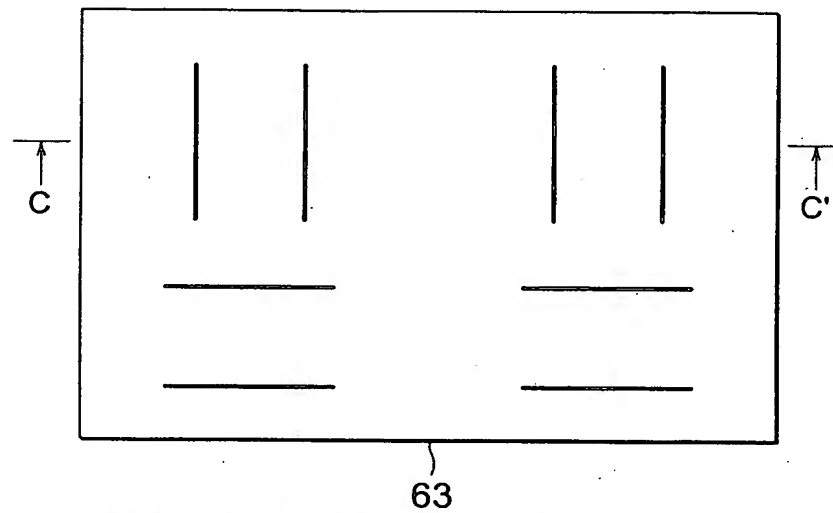


FIG. 5C (PRIOR ART)

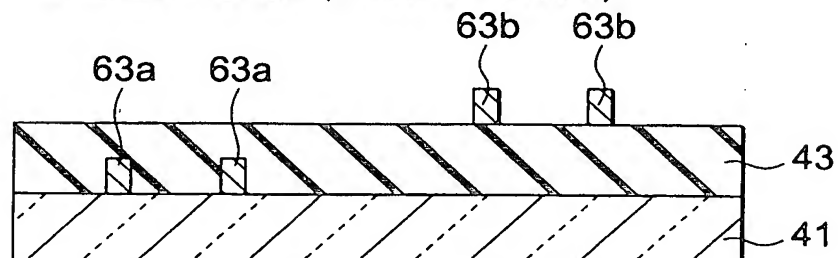


FIG. 6A
(PRIOR ART)

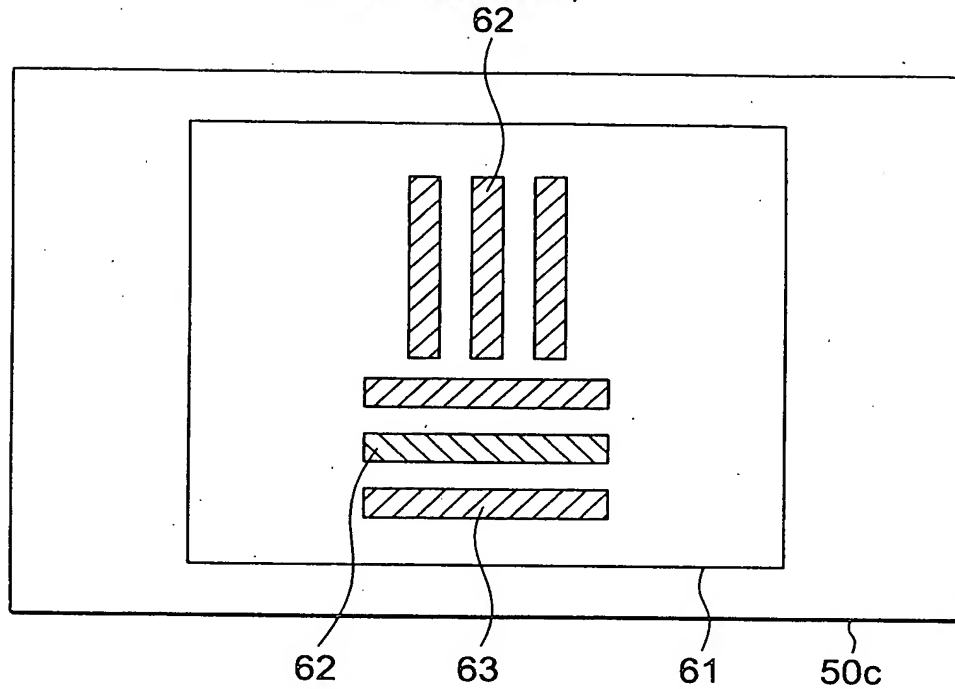


FIG. 6B
(PRIOR ART)

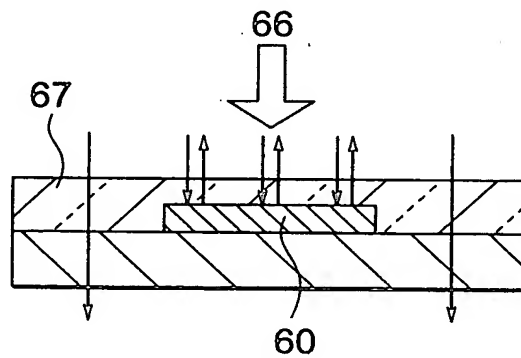


FIG. 6C
(PRIOR ART)

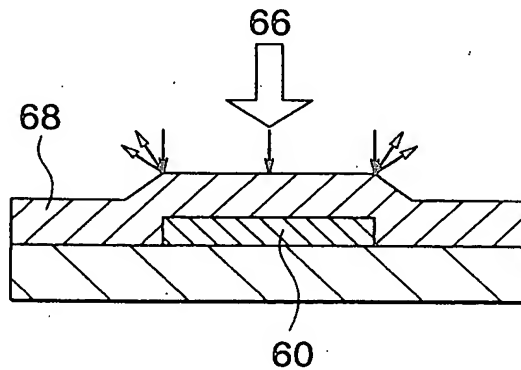


FIG. 7A
(PRIOR ART)

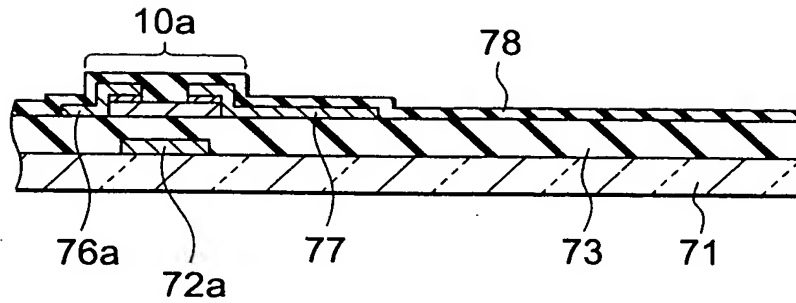


FIG. 7B
(PRIOR ART)

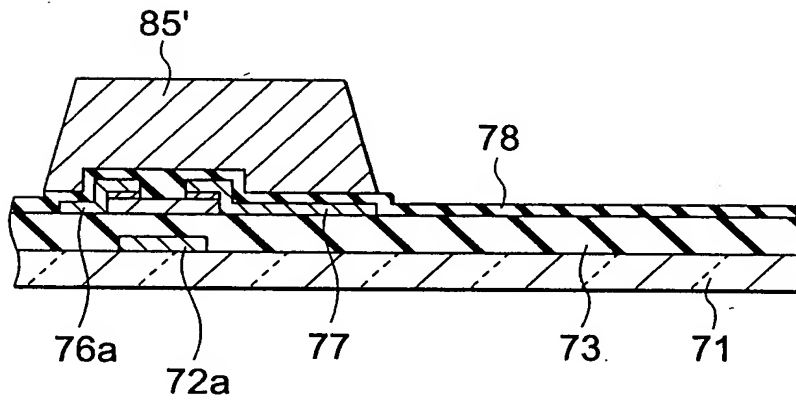


FIG. 7C
(PRIOR ART)

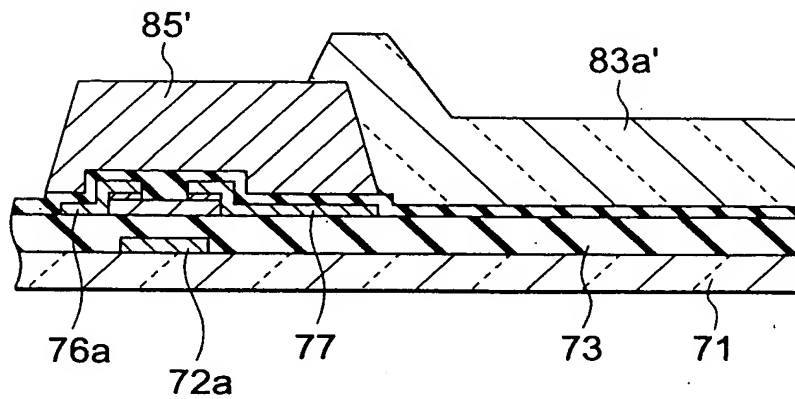


FIG. 8A
(PRIOR ART)

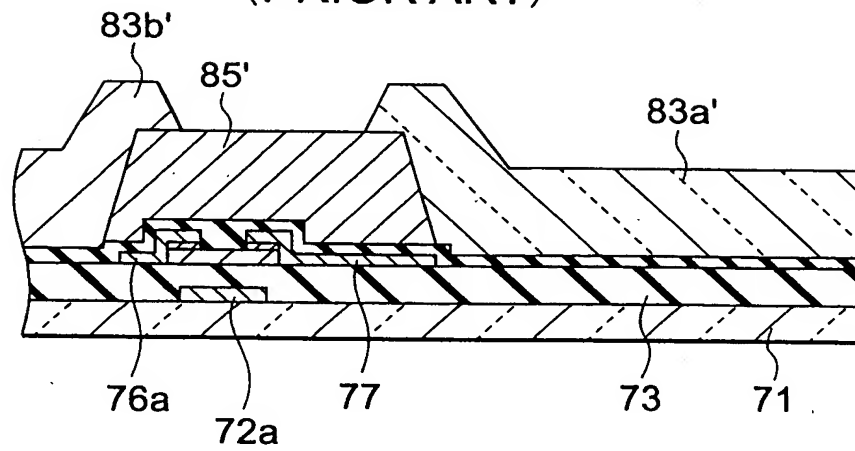


FIG. 8B
(PRIOR ART)

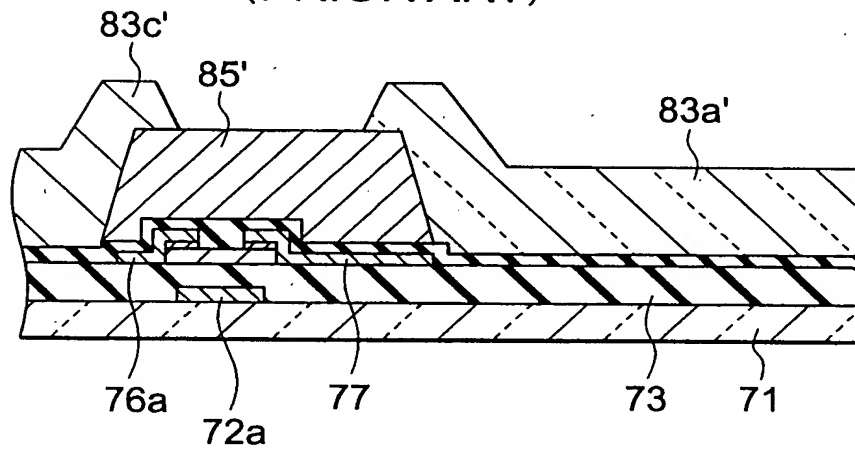


FIG. 8C
(PRIOR ART)

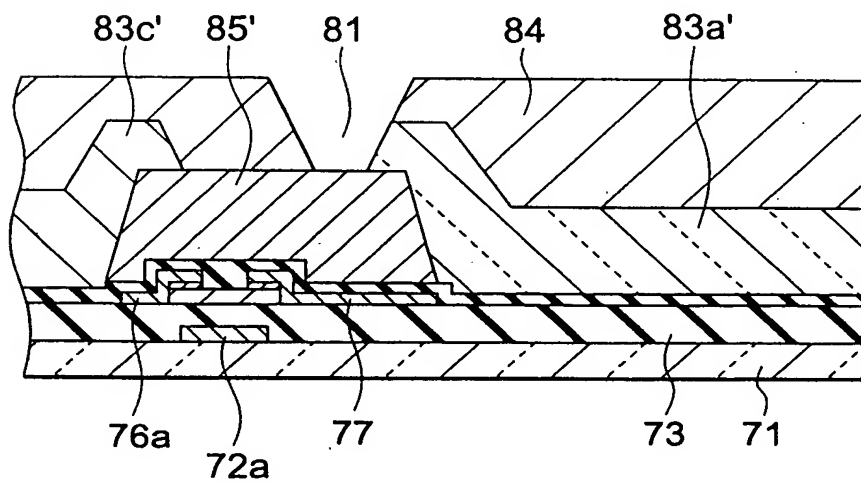


FIG. 9A
(PRIOR ART)

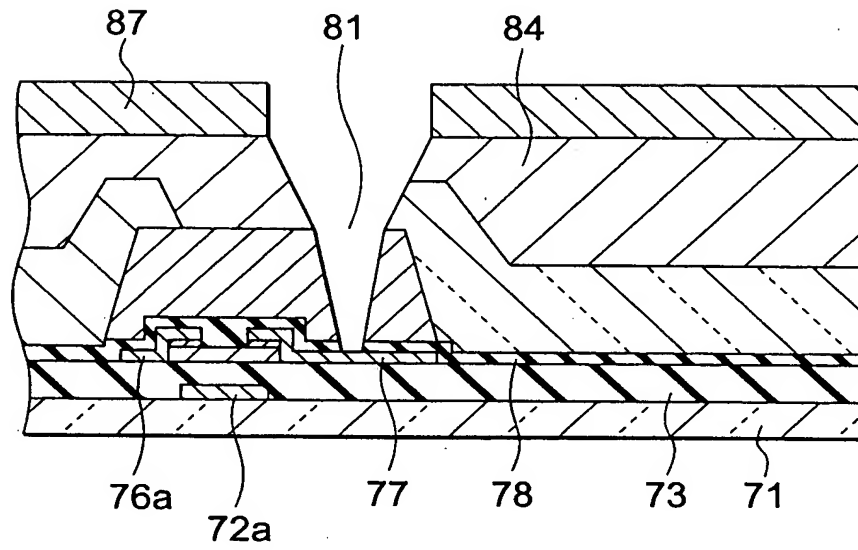


FIG. 9B
(PRIOR ART)

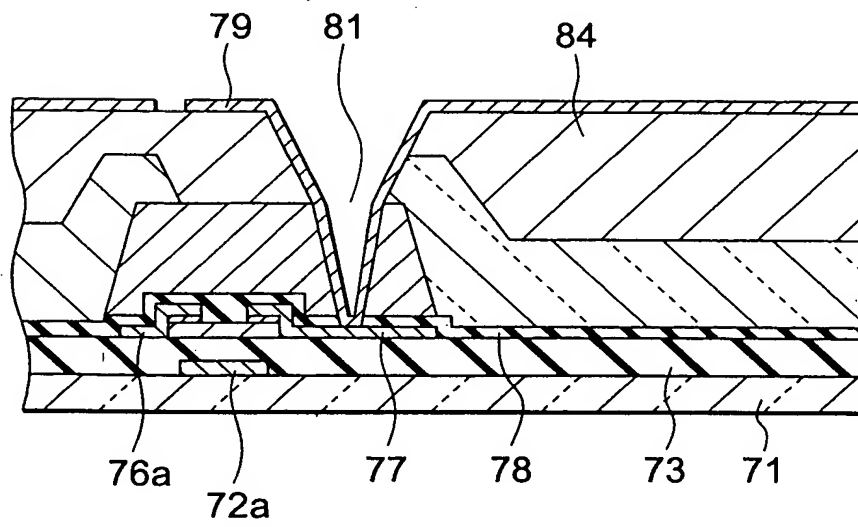


FIG. 10A
(PRIOR ART)

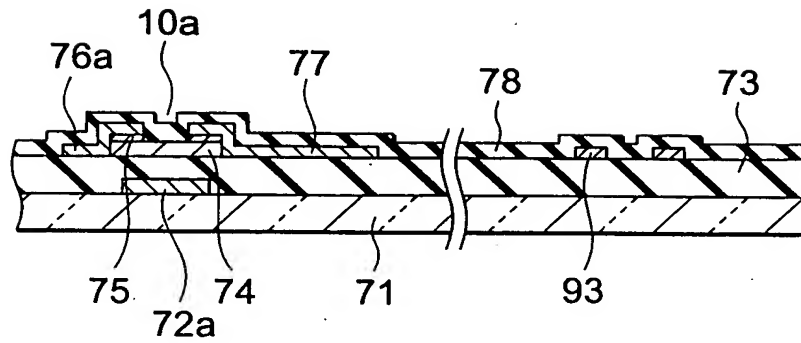


FIG. 10B
(PRIOR ART)

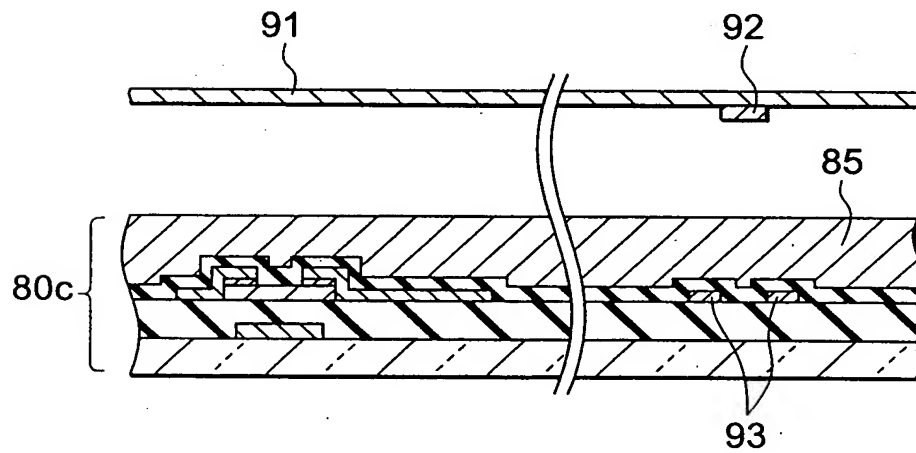


FIG. 10C
(PRIOR ART)

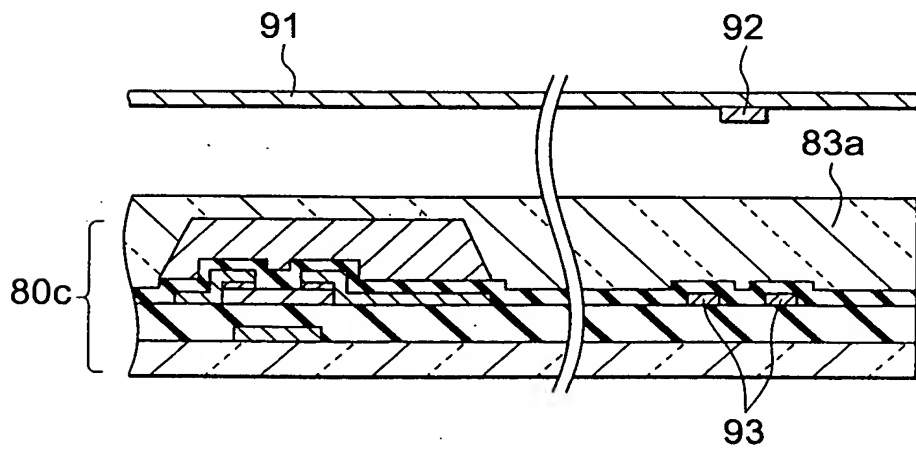


FIG. 11A
(PRIOR ART)

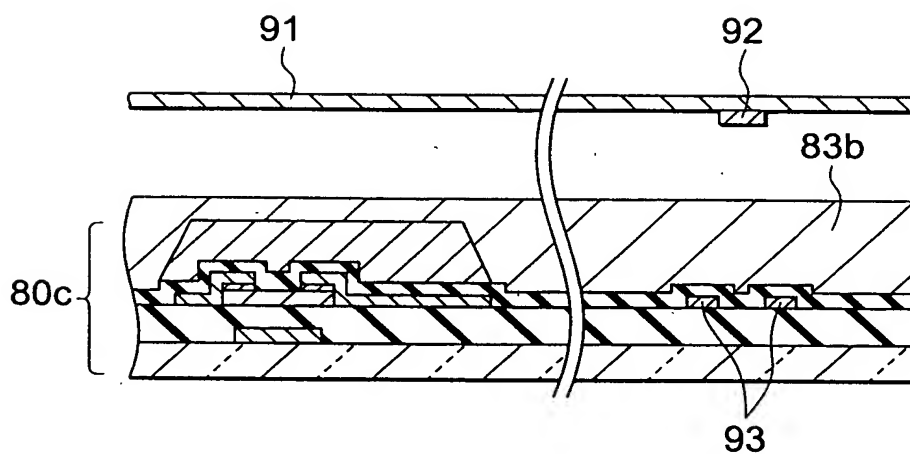


FIG. 11B
(PRIOR ART)

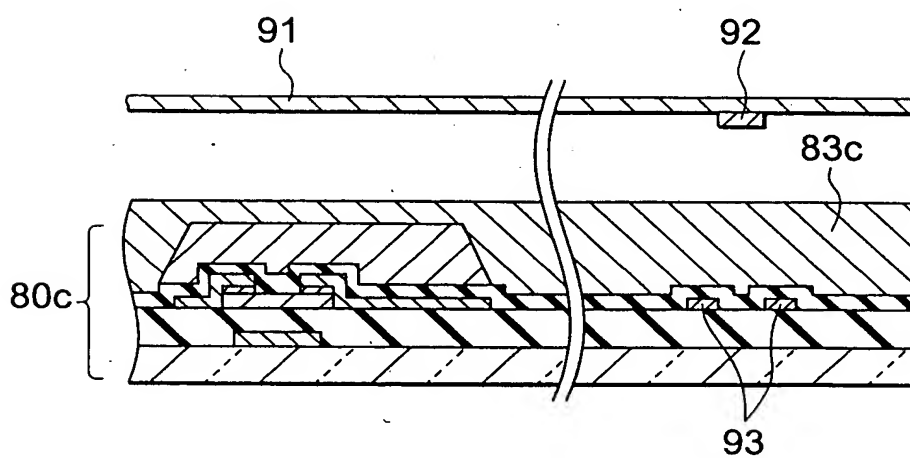


FIG. 12A
(PRIOR ART)

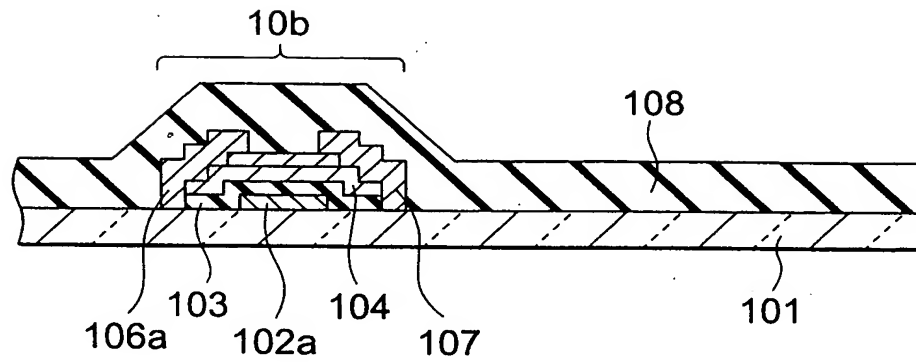


FIG. 12B
(PRIOR ART)

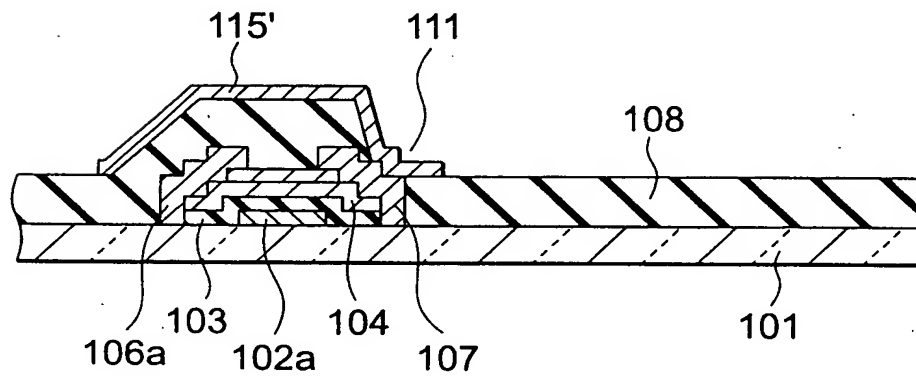


FIG. 12C
(PRIOR ART)

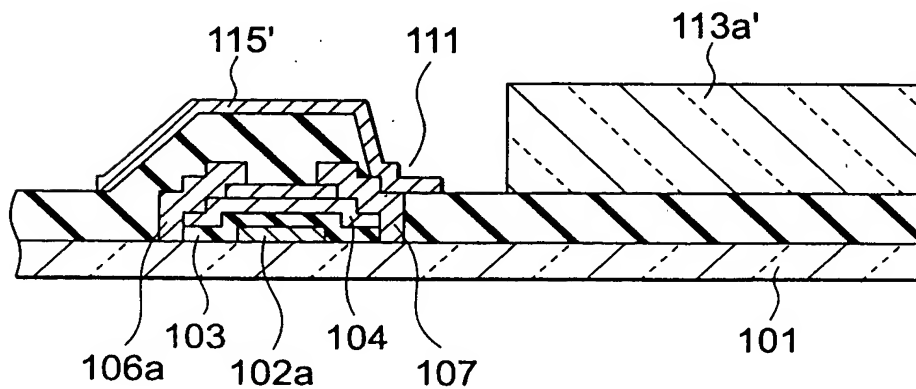


FIG. 13A
(PRIOR ART)

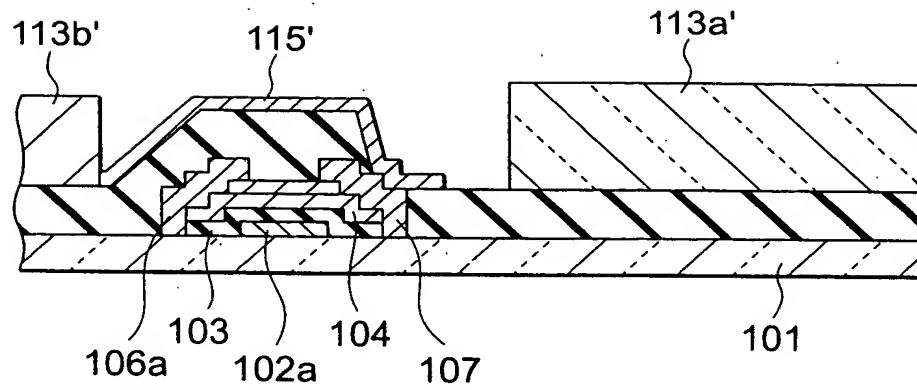


FIG. 13B
(PRIOR ART)

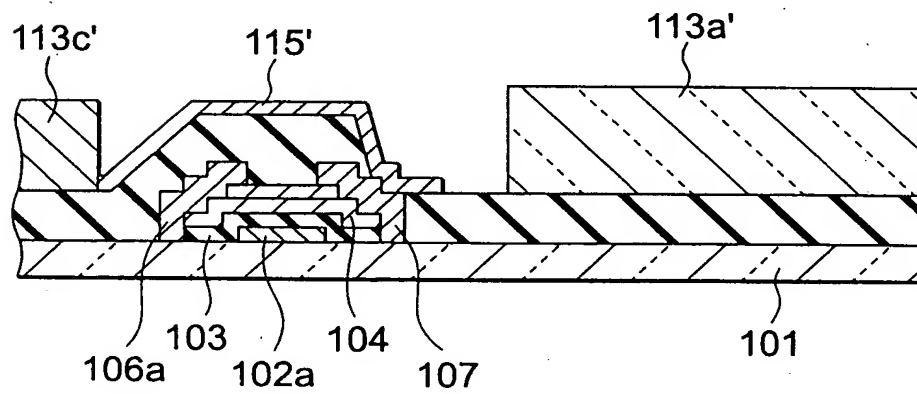


FIG. 13C
(PRIOR ART)

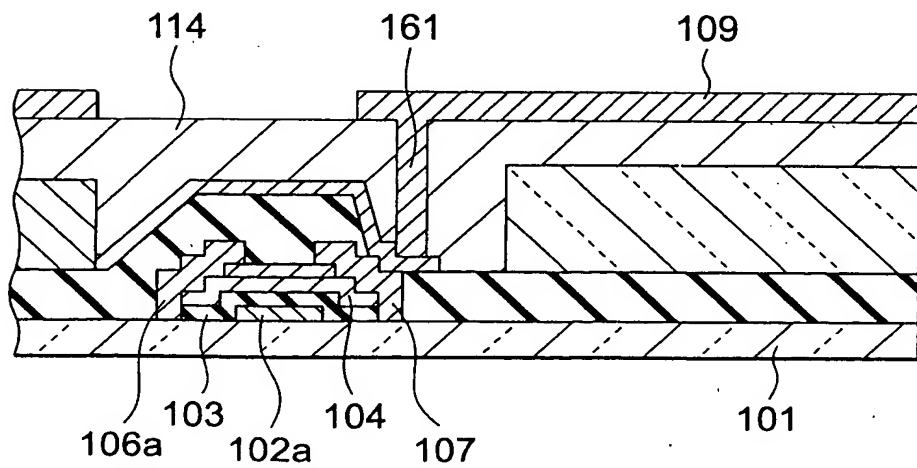


FIG. 14A
(PRIOR ART)

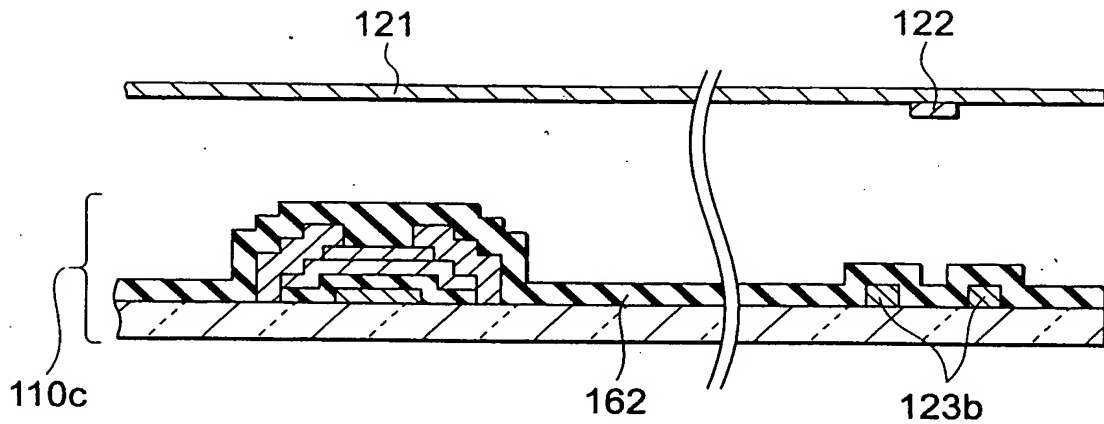


FIG. 14B
(PRIOR ART)

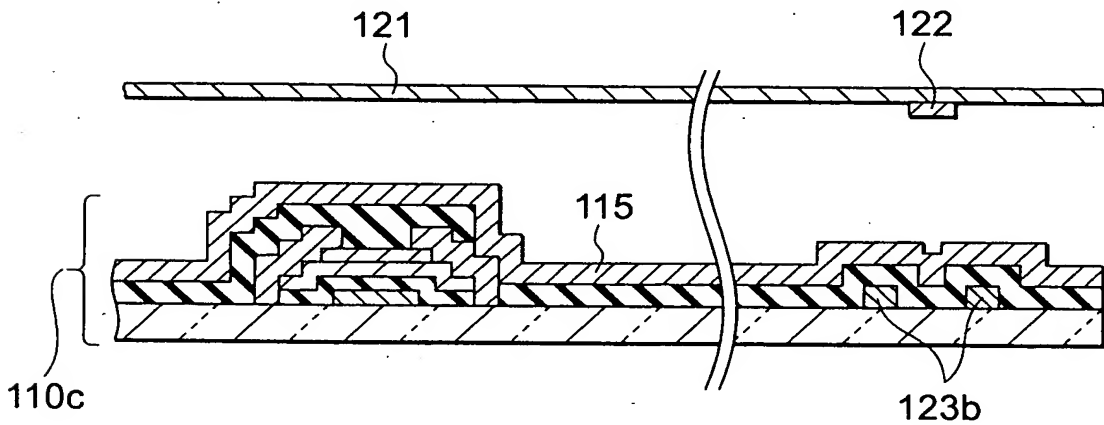


FIG. 14C
(PRIOR ART)

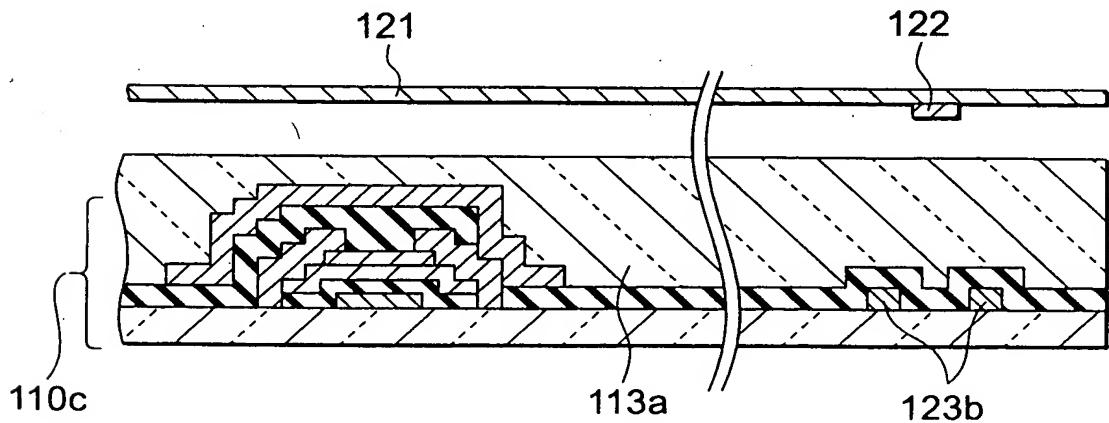


FIG. 15A
(PRIOR ART)

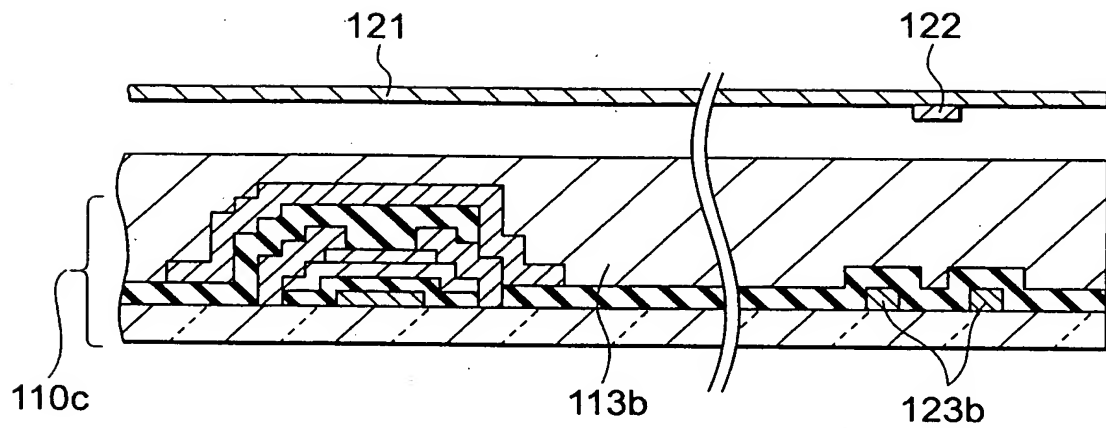


FIG. 15B
(PRIOR ART)

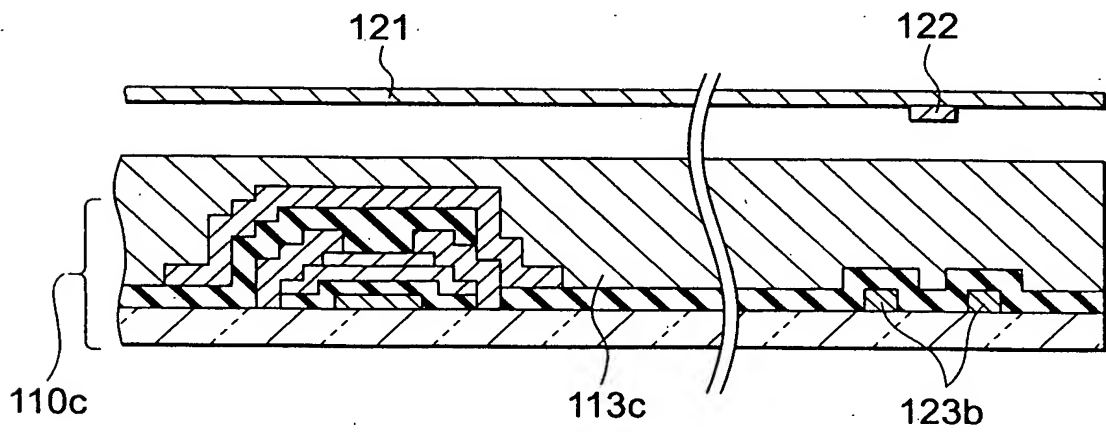


FIG. 16A
(PRIOR ART)

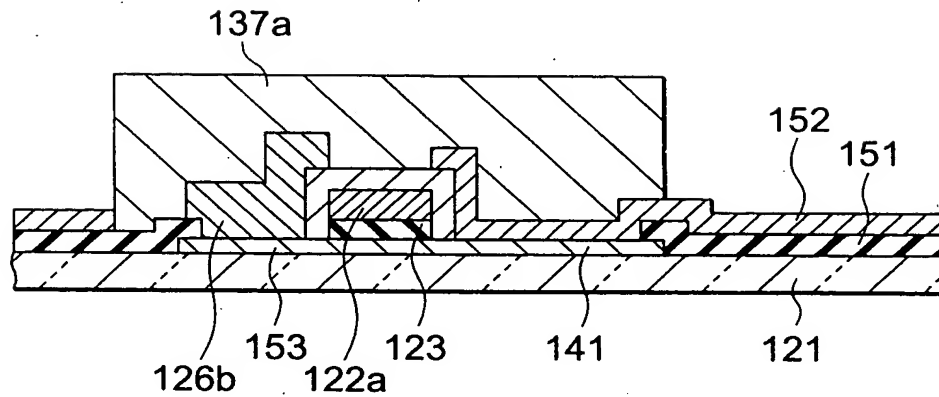


FIG. 16B
(PRIOR ART)

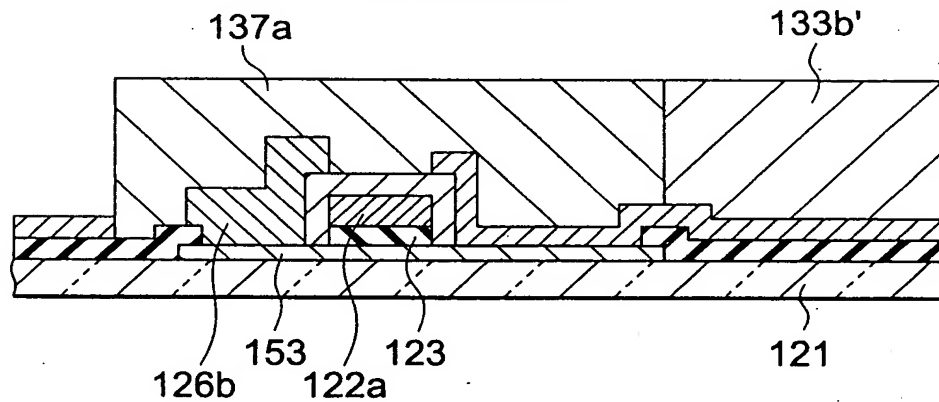


FIG. 16C
(PRIOR ART)

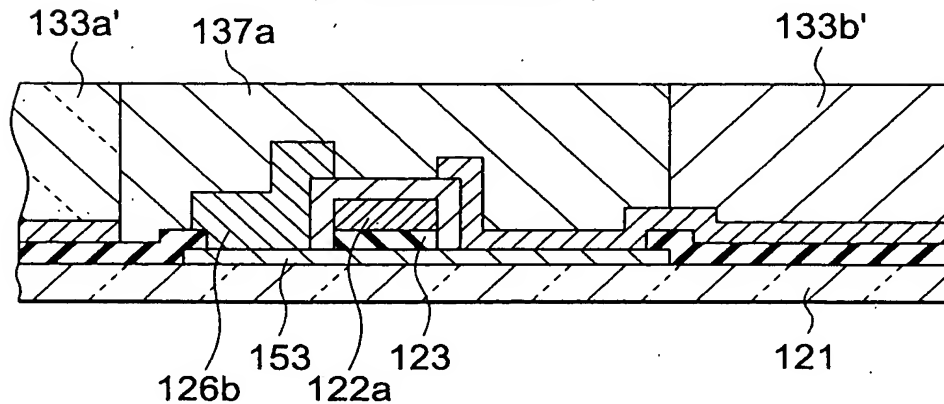


FIG. 17A
(PRIOR ART)

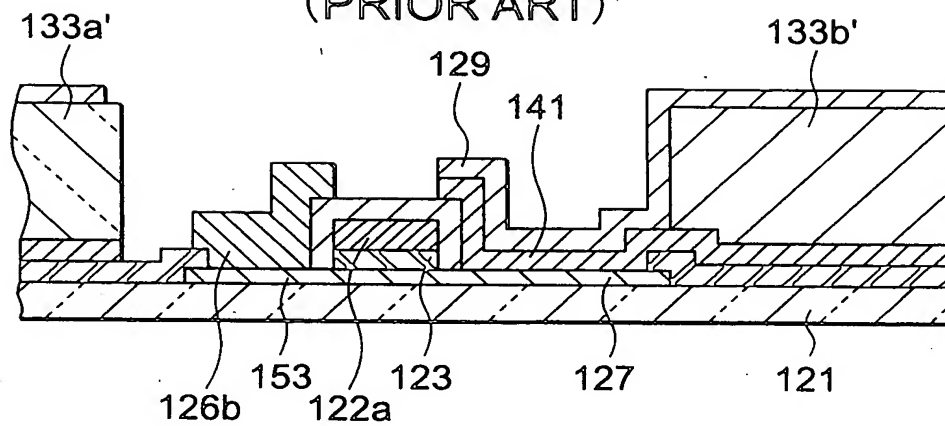


FIG. 17B
(PRIOR ART)

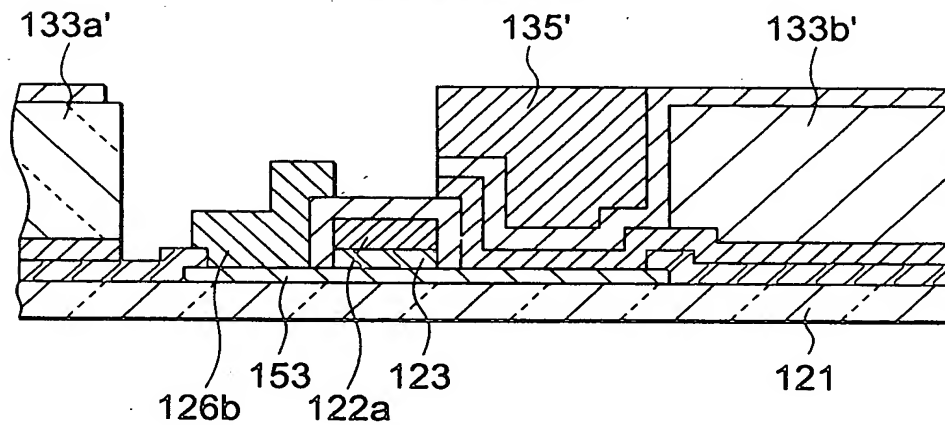


FIG. 17C
(PRIOR ART)

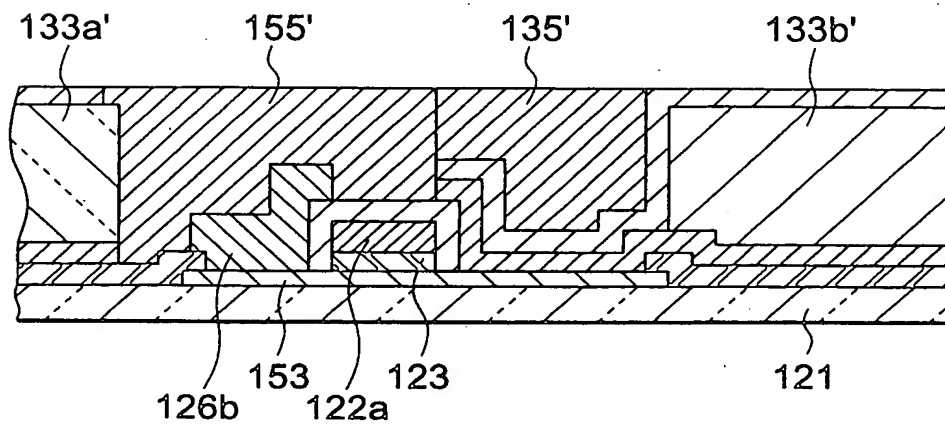


FIG. 18

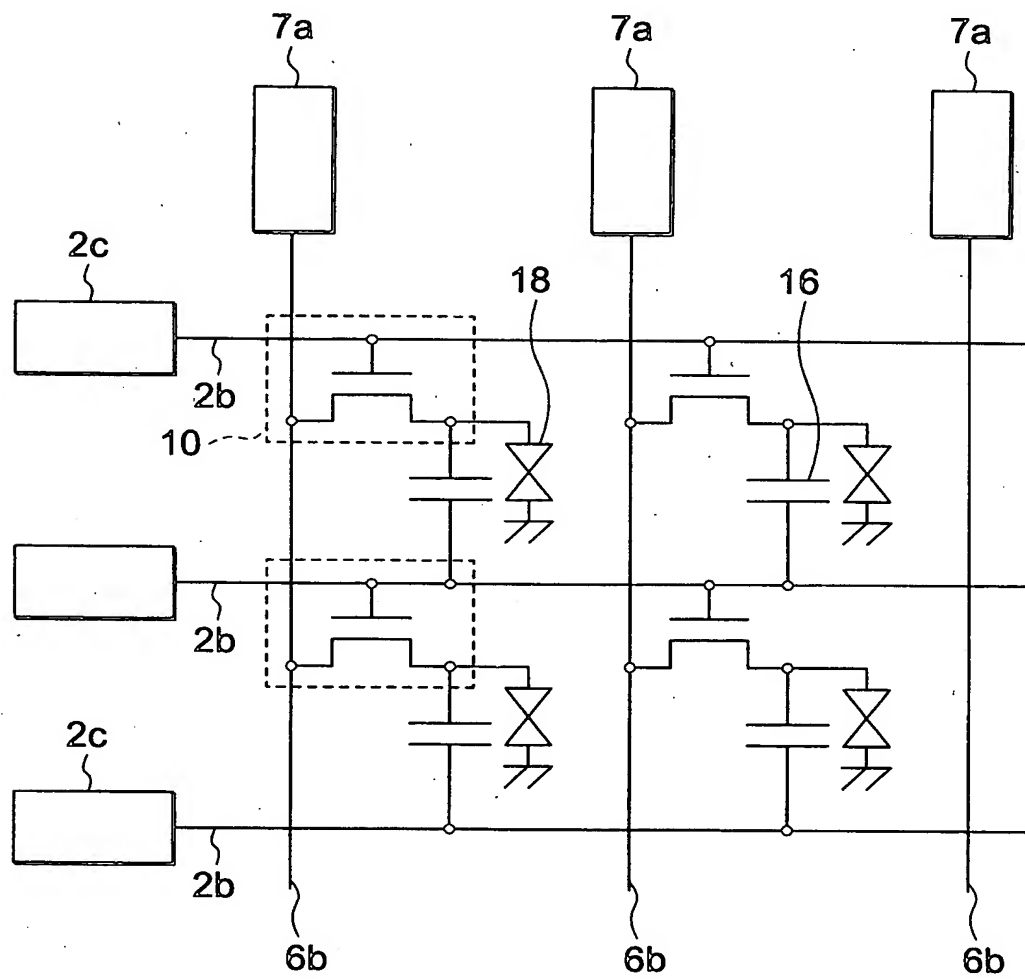


FIG. 19A

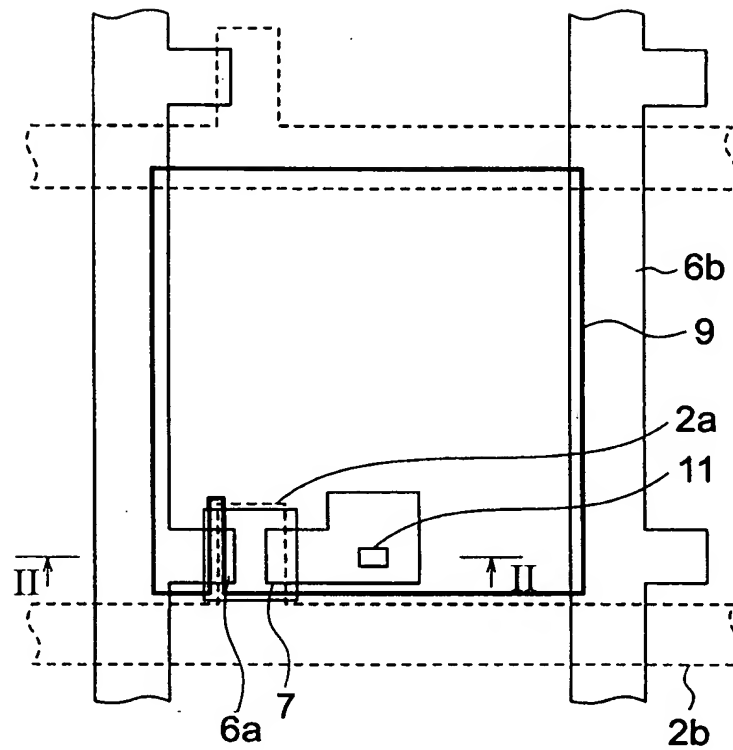


FIG. 19B

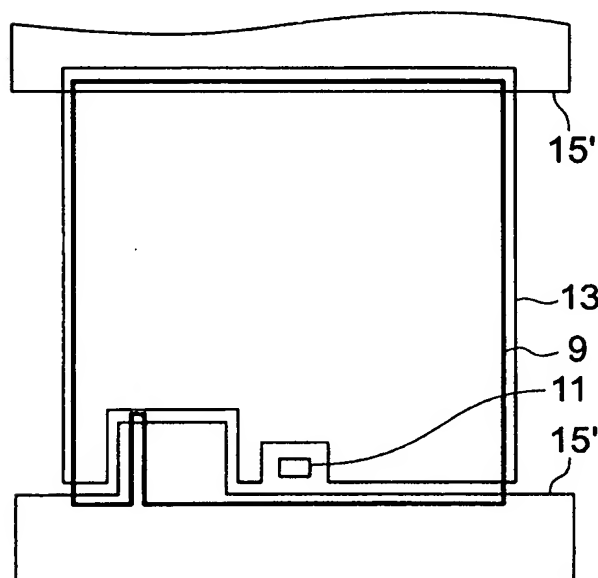


FIG. 20A

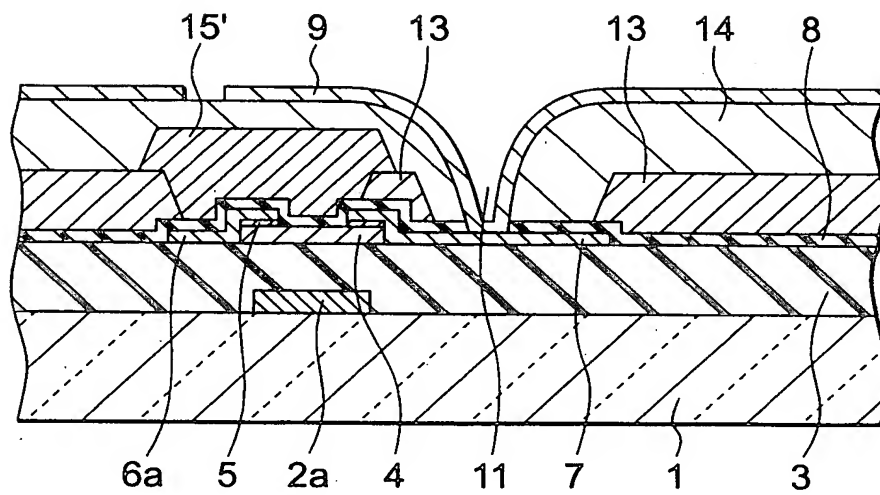


FIG. 20B

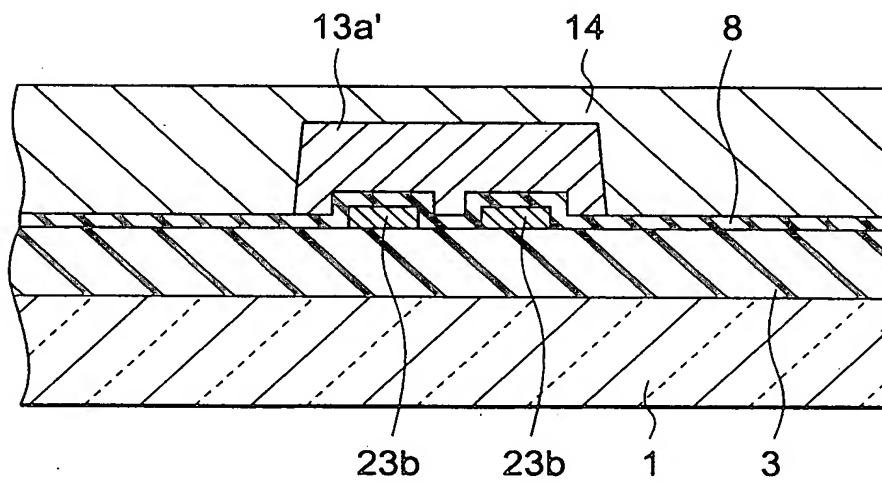


FIG. 21A

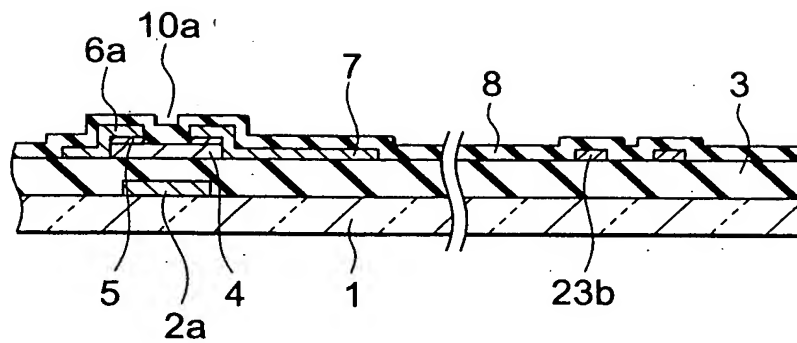


FIG. 21B

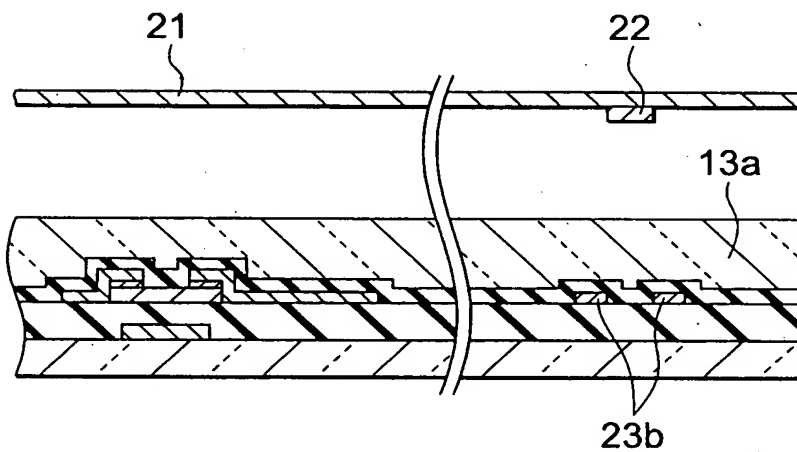


FIG. 21C

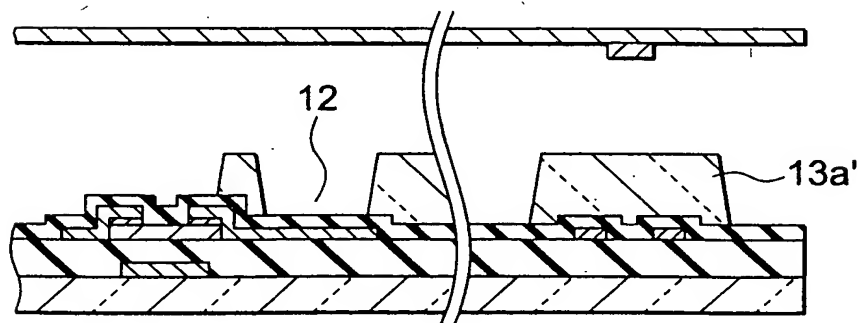


FIG. 22A

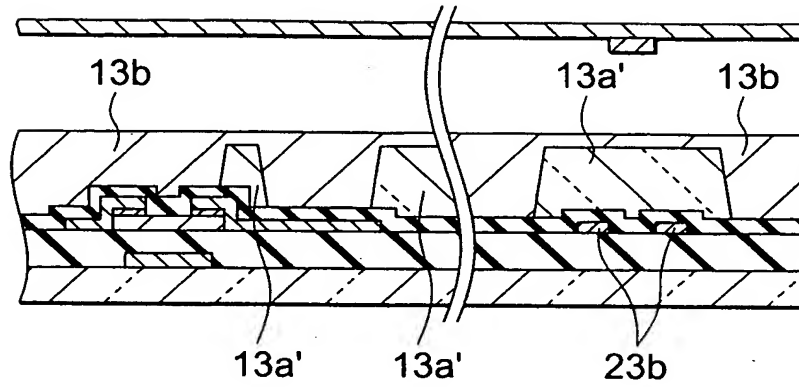


FIG. 22B

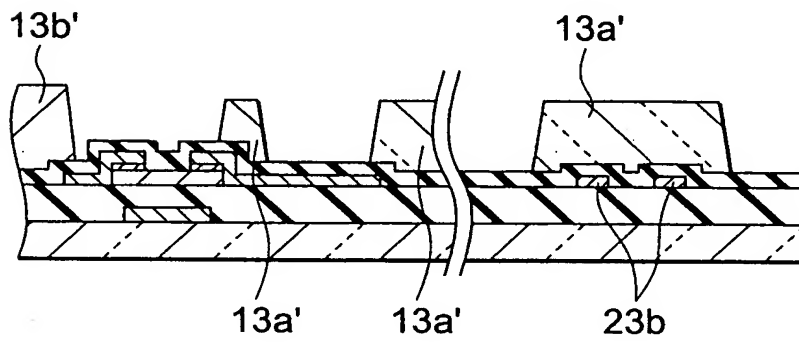


FIG. 22C

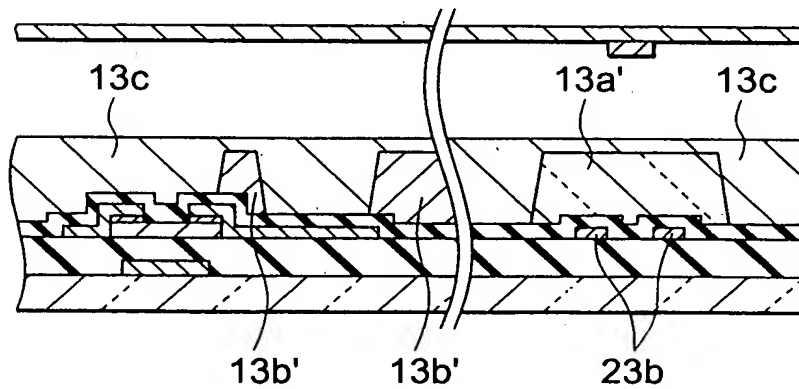


FIG. 23A

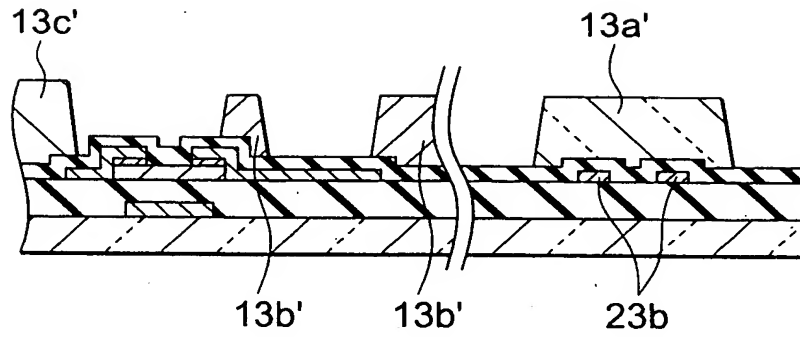


FIG. 23B

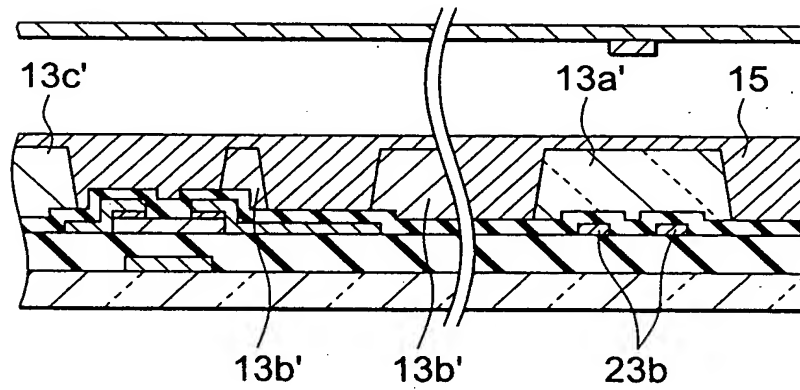


FIG. 23C

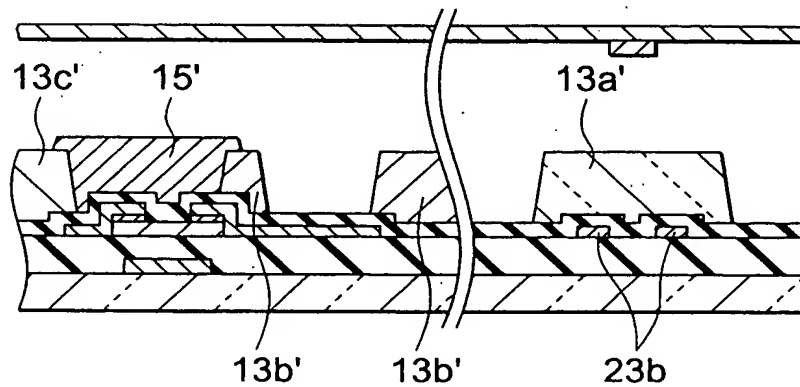


FIG. 24A

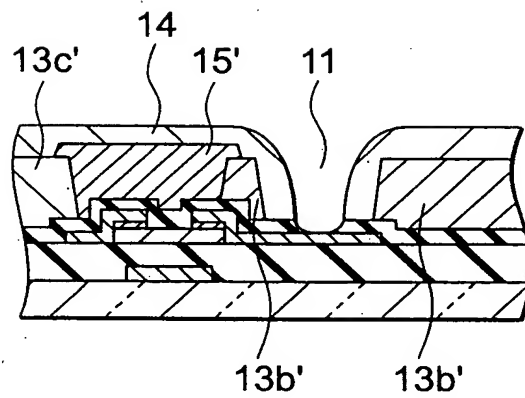


FIG. 24B

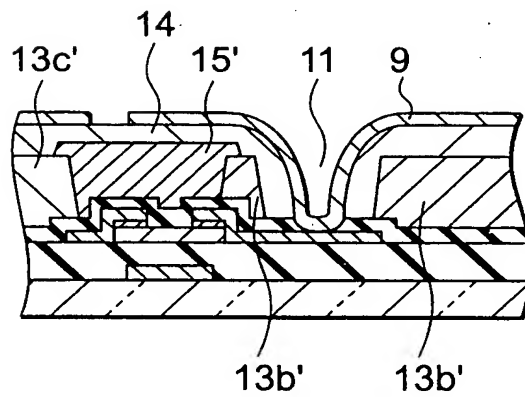


FIG. 25

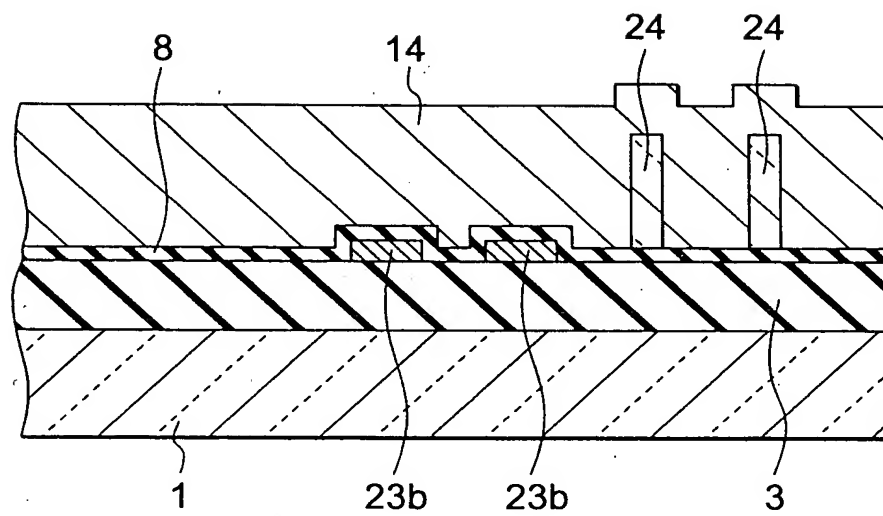


FIG. 26A

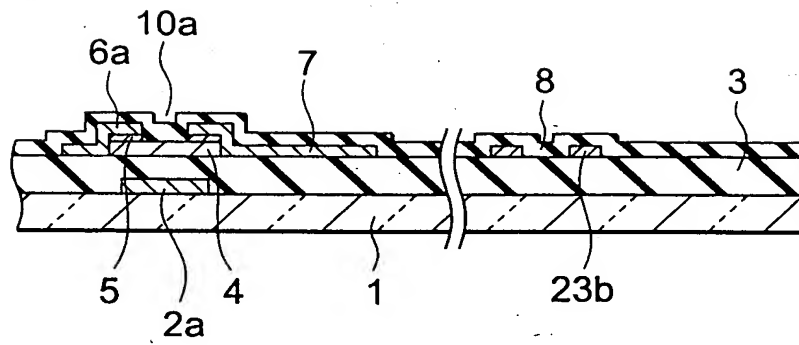


FIG. 26B

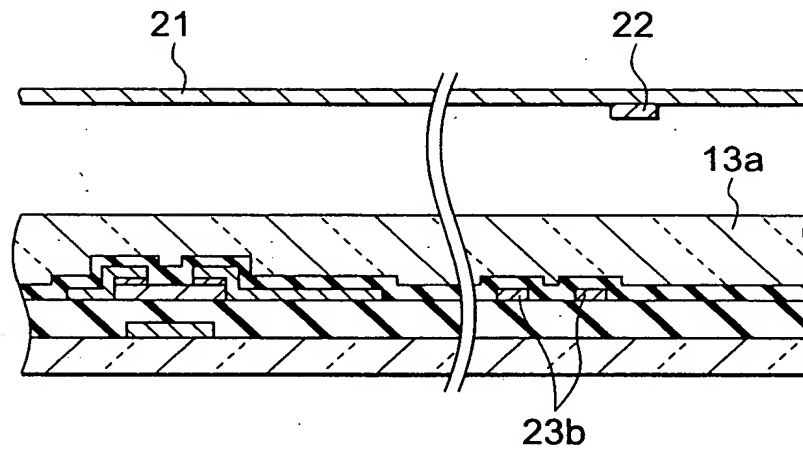


FIG. 26C

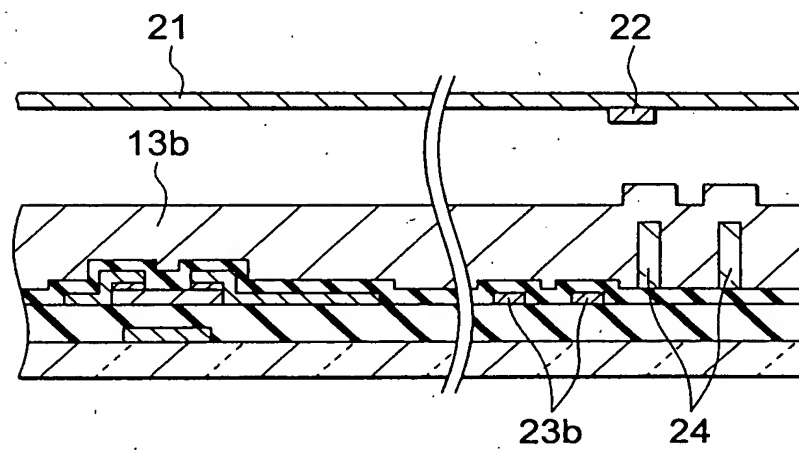


FIG. 27A

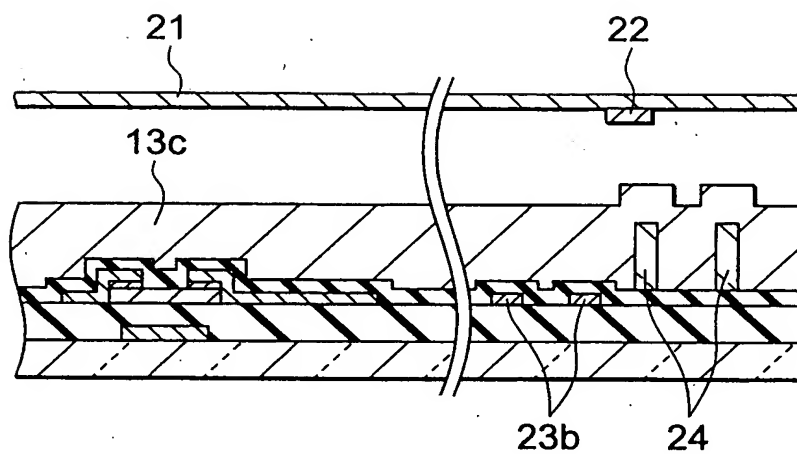


FIG. 27B

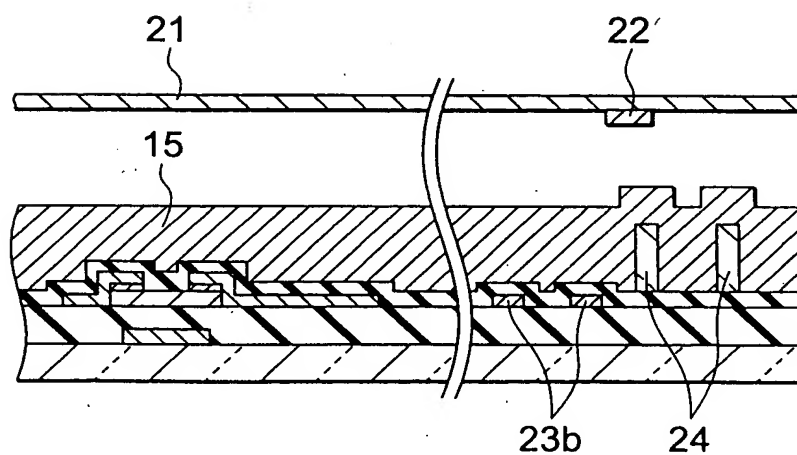


FIG. 28

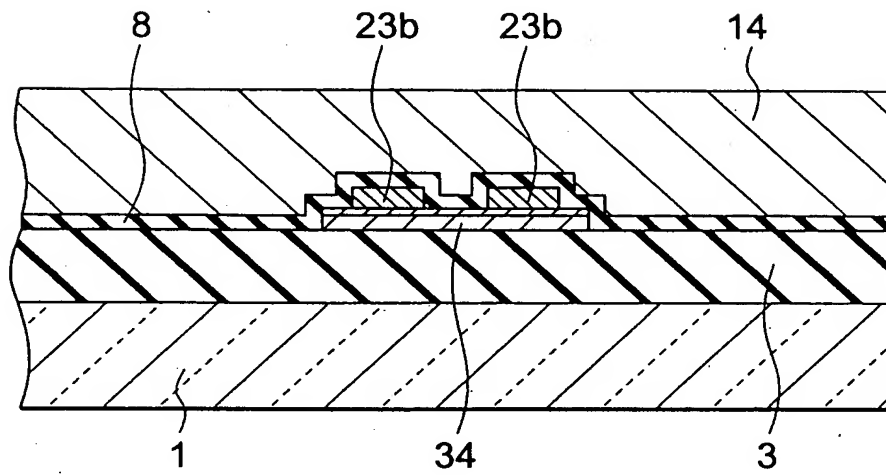


FIG. 29A

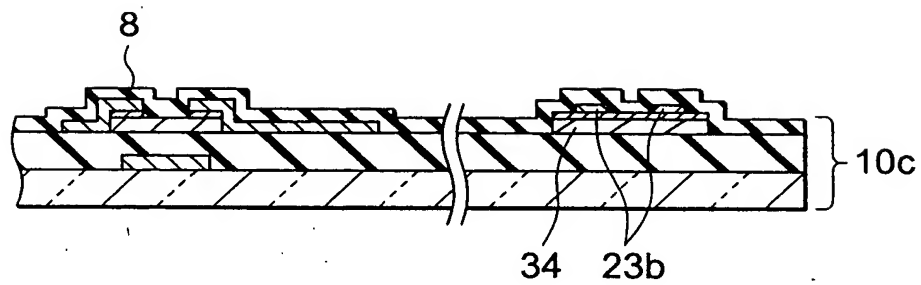


FIG. 29B

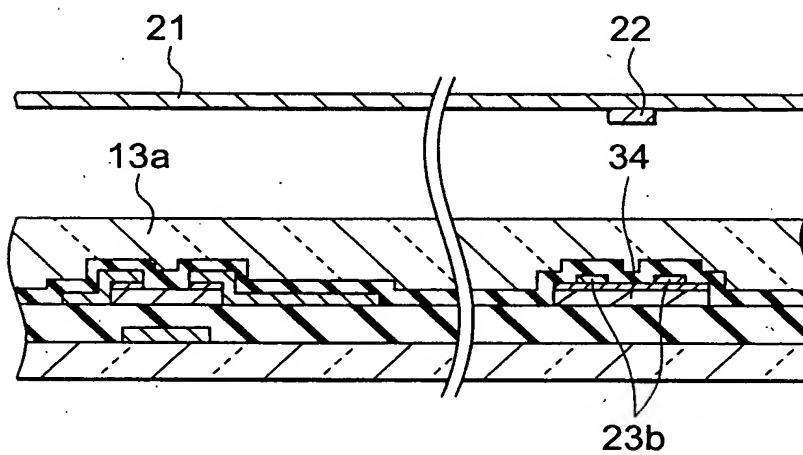


FIG. 29C

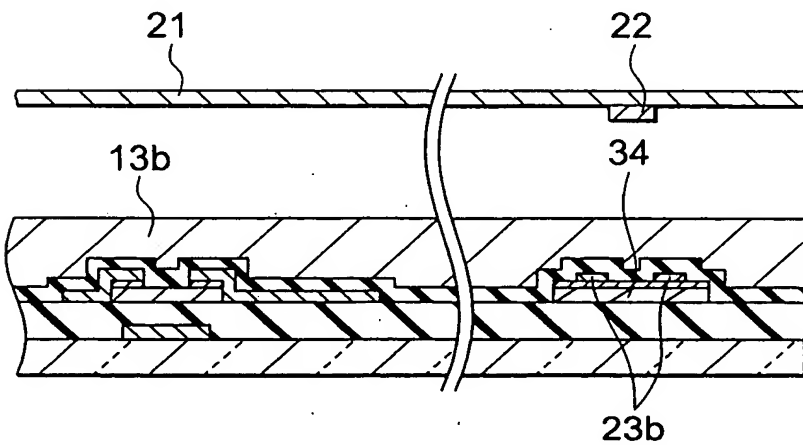


FIG. 30A

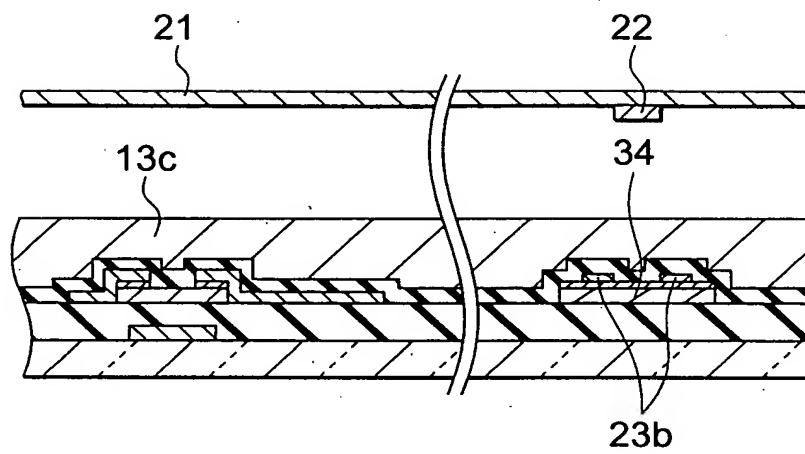


FIG. 30B

